Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VOUT**
2. **VOUT**
3. **VIN**
4. **NC**
5. **NC**
6. **NC**
7. **NC**
8. **ADJUST**

**.042”**

**8 7 6 5 4**

**1 2**

**3**

**317L**

**MASK**

**REF**

**.044”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .0035 x .0035”**

**Backside Potential: Connect Chip Back to VOUT**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .042” X .044” DATE: 2/27/23**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: LM317L**

**DG 10.1.2**

#### Rev B, 7/1